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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/758,540	01/10/2001	Harish R. Devanagondi	CISCO-2039	9394

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/758,540	DEVANAGONDI ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on August 30, 2005. This amendment has been entered and carefully considered. Claims 1, 3, 8, 10, 15, 22, 24, 29, 31 and 33 are amended and claims 1-37 are again presented for examination.

2. Applicant's arguments filed on August 30, 2005 have been fully considered but they are deemed to be moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Homewood et al. (USPN: 6,807,628) hereinafter Homewood.

As per claim 1, Homewood teaches an apparatus for exception handling in a data packet processor (the data processor, 100 in Figs. 1-2 and 4), comprising:

- a packet processing pipeline (the instruction execution pipeline, 400 in Fig. 4) including at least two processing stages (401-407 in Fig. 4) for processing a sequential (i.e. each instruction passes sequentially through each pipeline stage in order to complete its execution) plurality of data

packets (instructions), each of the plurality of data packets having an exception map (other than instruction bits in 128-bit wide words stored in the instruction cache, 215 in Fig. 2) associated therewith (e.g. see the abstract, claim 1, Col. 2, lines 10-12 and Figs. 1-2 and 4), wherein the exception map has one or more entries, each of the entries associated with a particular exception condition (e.g. see Col. 7, lines 38-44);

- an exception detector (the interrupt and exception controller, 240 in Figs. 2 and 5) associated with each of the processing stages, the detector detecting whether any of a plurality of exception conditions applies/associated to a data packet (e.g. see Col. 7, lines 38-44 and Figs. 2 and 5); and
- a bit setter responsive to the exception detector to set, modify, or reset at least one of the entries (a valid stop bit) of an exception map associated with the data packet (e.g. see Col. 12, line 45).

The further limitation of processing the execution map, by an exception handler, at a stage later than a stage in which the bit setter has set, modified or reset one of the entries is an inherent feature because in the pipeline processing taught by Homewood, if one of the entries is set, modified or reset in a particular/current stage, then processing of that modification has to be handled/processed in the next/following stage.

As per claim 2, Homewood teaches the claimed invention as described above and furthermore, Homewood teaches that each of the exception conditions further

comprise a plurality of logical operations, i.e. the arithmetic or load/store operations (e.g. see Col. 8, lines 12-16).

As per claim 3, Homewood teaches the claimed invention as described above and furthermore, Homewood teaches that the apparatus further comprising an exception handler to process the exception map in response to the entries that are set in the exception map when all of the processing stages are complete, i.e. by generating exception in response to the exception condition upon completed execution of earlier ones of the executing instructions (e.g. see the abstract and the claim 1).

As per claim 4, Homewood teaches the claimed invention as described above and furthermore, Homewood teaches that the apparatus further comprising a memory (the instruction cache, 215 in Fig. 2) associated with the data packet to store the exception map (other than instruction bits in 128-bit wide words stored in the instruction cache, 215 in Fig. 2).

As per claims 8, 15, 22, 29 and 31, refer arguments with respect to the rejection of claim 1 above. These claims are rejected based on the same rationale as the rejection of claim 1.

As per claims 6, 9, 13, 16, 20, 23, 27, 32 and 36, refer arguments with respect to the rejection of claim 2 above. These claims are rejected based on the same rationale as the rejection of claim 2.

As per claims 5, 10, 12, 17, 19, 24, 26, 30, 33 and 35, refer arguments with respect to the rejection of claim 3 above. These claims are rejected based on the same rationale as the rejection of claim 3.

As per claims 7, 11, 14, 18, 21, 25, 28, 34 and 37, refer arguments with respect to the rejection of claim 4 above. These claims are rejected based on the same rationale as the rejection of claim 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Homewood in view of Dean (USPN: 5,544,342).

As per claim 1, Homewood teaches an apparatus for exception handling in a data packet processor (the data processor, 100 in Figs. 1-2 and 4), comprising:

- a packet processing pipeline (the instruction execution pipeline, 400 in Fig. 4) including at least two processing stages (401-407 in Fig. 4) for processing a sequential (i.e. each instruction passes sequentially through each pipeline stage in order to complete its execution) plurality of data packets (instructions), each of the plurality of data packets having an exception map (other than instruction bits in 128-bit wide words stored in the instruction cache, 215 in Fig. 2) associated therewith (e.g. see the abstract, claim 1, Col. 2, lines 10-12 and Figs. 1-2 and 4), wherein the

exception map has one or more entries, each of the entries associated with a particular exception condition (e.g. see Col. 7, lines 38-44);

- an exception detector (the interrupt and exception controller, 240 in Figs. 2 and 5) associated with each of the processing stages, the detector detecting whether any of a plurality of exception conditions applies/associated to a data packet (e.g. see Col. 7, lines 38-44 and Figs. 2 and 5); and
- a bit setter responsive to the exception detector to set, modify, or reset at least one of the entries (a valid stop bit) of an exception map associated with the data packet (e.g. see Col. 12, line 45).

As explained above, the further limitation of processing the execution map, by an exception handler, at a stage later than a stage in which the bit setter has set, modified or reset one of the entries is an inherent feature because in the pipeline processing taught by Homewood, if one of the entries is set, modified or reset in a particular/current stage, then processing of that modification has to be handled/processed in the next/following stage. Even if it is not true, Dean teaches this limitation of processing/handling the exception at the next stage/cycle to avoid irreparable changes to the processor's state (e.g. see Col. 59, line 47 – Col. 60, line 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Dean in the apparatus taught by Homewood so irreparable changes to the processor's state are avoided.

As per claim 2, the combination of Homewood and Dean teaches the claimed invention as described above and furthermore, Homewood teaches that each of the exception conditions further comprise a plurality of logical operations, i.e. the arithmetic or load/store operations (e.g. see Col. 8, lines 12-16).

As per claim 3, the combination of Homewood and Dean teaches the claimed invention as described above and furthermore, Homewood teaches that the apparatus further comprising an exception handler to process the exception map in response to the entries that are set in the exception map when all of the processing stages are complete, i.e. by generating exception in response to the exception condition upon completed execution of earlier ones of the executing instructions (e.g. see the abstract and the claim 1).

As per claim 4, the combination of Homewood and Dean teaches the claimed invention as described above and furthermore, Homewood teaches that the apparatus further comprising a memory (the instruction cache, 215 in Fig. 2) associated with the data packet to store the exception map (other than instruction bits in 128-bit wide words stored in the instruction cache, 215 in Fig. 2).

As per claims 8, 15, 22, 29 and 31, refer arguments with respect to the rejection of claim 1 above. These claims are rejected based on the same rationale as the rejection of claim 1.

As per claims 6, 9, 13, 16, 20, 23, 27, 32 and 36, refer arguments with respect to the rejection of claim 2 above. These claims are rejected based on the same rationale as the rejection of claim 2.

As per claims 5, 10, 12, 17, 19, 24, 26, 30, 33 and 35, refer arguments with respect to the rejection of claim 3 above. These claims are rejected based on the same rationale as the rejection of claim 3.

As per claims 7, 11, 14, 18, 21, 25, 28, 34 and 37, refer arguments with respect to the rejection of claim 4 above. These claims are rejected based on the same rationale as the rejection of claim 4.

Remarks

5. As to the remark, Applicant asserted that independent claims 5, 12, 19, 26 and 35 already contain a limitation as to the fact that "the execution map is utilized at a later stage than when the bit is set".

Examiner respectfully traverses Applicant's remark because none of independent claims 5, 12, 19, 26 and 35 contain this limitation.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER